

What is claimed is:

1. An evolvable circuit, comprising:

a plurality of transistors, each of said transistors
5 comprising a first power terminal, a second power terminal and a control terminal;

a plurality reconfigurable switches, each single one of
said switches providing an individual interruptable terminal-to-
terminal connection among said transistors, said plurality of
10 reconfigurable switches comprising:

a first plurality of reconfigurable switches
connected to form a first series-connected succession of said
transistors, whereby each pair of successive transistors in said
succession have a connection at the first power terminal of one
15 transistor and the second power terminal of the other transistor
of the pair through a corresponding single reconfigurable switch,
each connection being governed by the corresponding single
reconfigurable switch.

20 2. The circuit of Claim 1 wherein the number of said
transistors exceeds three and the number of said reconfigurable
switches is within an order of magnitude of the number of
terminals of said plurality of transistors, said number of
terminals including said first power terminals, said second power
25 terminals and said control terminals of said plurality of
transistors.

3. The circuit of Claim 2, wherein said plurality of
reconfigurable switches comprises reconfigurable switches having
30 variable conductance states.

4. The evolvable circuit of Claim 1 wherein said plurality

of reconfigurable switches further comprises:

a second plurality of reconfigurable switches connected between the first power terminals of respective pairs of said transistors.

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5. The evolvable circuit of Claim 4 wherein said plurality of reconfigurable switches further comprises:

a third plurality of reconfigurable switches, each respective one of which is connected between the control terminal and said first power terminal of a respective one of said transistors.

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6. The circuit of Claim 5 wherein said first plurality of reconfigurable switches forms plural respective series-connected successions of transistors that are parallel to one another, and wherein said plurality of reconfigurable switches further comprises:

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a fourth plurality of reconfigurable switches each connected between the control terminals of a pair of corresponding ones of the transistors in different ones of said series-connected successions of transistors.

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7. The circuit of Claim 6 wherein said plural series-connected successions of transistors are arranged in columns of transistors, the corresponding transistors in different columns forming rows of transistors, the transistors in a first plurality of said rows being of a first conductivity type and the transistors in the remaining ones of said rows being of a second conductivity type complementary to said first conductivity type.

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8. The circuit of Claim 6 wherein said plurality of

reconfigurable switches further comprises:

a fifth plurality of reconfigurable switches connected between one of said first and second power terminals of the transistors of different ones of said series-connected

5 successions of transistors.

9. The circuit of Claim 8 wherein said plurality of reconfigurable switches further comprises:

10 a reconfigurable switch connected between the first power terminal of a transistor in one of said series-connected successions of transistors and the second power terminal of a transistor of a different one of said series-connected successions of transistors.

15 10. An evolvable circuit comprising:

a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal;

20 a plurality reconfigurable switches, each single one of said reconfigurable switches providing an individual interruptable terminal-to-terminal connection in said plurality of transistors; and

all terminal-to-terminal connections among said plurality of transistors being provided through respective ones of said plurality of reconfigurable switches with the exception of connections through voltage sources.

11. The circuit of Claim 10 wherein the number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power terminals and said control terminals of said plurality of

transistors.

12. The circuit of Claim 11, wherein the number of said reconfigurable switches is at least nearly the same as the number of terminals of said plurality of transistors.

13. An evolvable circuit comprising:

• a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal;

a plurality reconfigurable switches, each single one of said reconfigurable switches providing an individual interruptable terminal-to-terminal connection in said plurality of transistors; and

wherein the number of said reconfigurable switches exceeds three and the number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power terminals and said control terminals of said plurality of transistors.

14. The circuit of Claim 13, wherein the number of said reconfigurable switches is at least nearly the same as the number of terminals of said plurality of transistors.

15. The circuit of Claim 13 wherein said plurality of reconfigurable switches comprise reconfigurable switches having variable conductances.

16. A circuit functioning successively in two modes including a configuration mode in which the topology of said circuit is modifiable and an operation mode in which the topology

of said circuit is fixed, said circuit comprising:

a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal, the states of said transistors changing during
5 said operation mode;

a plurality reconfigurable switches whose states are modifiable in accordance with an evolutionary algorithm in said configuration mode and fixed in said operation mode, each single one of said reconfigurable switches providing an individual
10 interruptable terminal-to-terminal connection between a respective pair of said transistors whereby one transistor is isolatable from another adjacent transistor, and defining an instantaneous topology of said circuit.

15 17. The circuit of Claim 16, wherein the number of said transistors exceeds three and the number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power
20 terminals and said control terminals of said plurality of transistors.

18. The circuit of Claim 17, wherein the number of said reconfigurable switches is about the same as the number of
25 terminals of said plurality of transistors.

19. The circuit of Claim 16 wherein said plurality of reconfigurable switches comprises:

a first plurality of reconfigurable switches connected
30 to form a first series-connected succession of said transistors, whereby each pair of successive transistors in said succession have a connection at the first power terminal of one transistor

and the second power terminal of the other transistor of the pair through a corresponding single reconfigurable switch, each connection being governed by the corresponding single reconfigurable switch.

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20. The circuit of Claim 16 wherein said plurality of reconfigurable switches comprises reconfigurable switches having variable conductances.